



ST7FLITE0

8-BIT MCU WITH SINGLE VOLTAGE FLASH MEMORY, DATA EEPROM, ADC, TIMERS, SPI

DATA BRIEFING

■ Memories

- 1.5K bytes single voltage Flash Program memory with read-out protection, In-Circuit Programming and In-Application Programming (ICP and IAP). 10K write/erase cycles guaranteed
- 128 bytes RAM
- 128 bytes data EEPROM with read-out protection. 300K write/erase cycles guaranteed

■ Clock, Reset and Supply Management

- 3-level low voltage supervisor (LVD) and auxiliary voltage detector (AVD) for safe power-on/off procedures
- Clock sources: internal 1MHz RC 1% oscillator or external clock
- Optional PLL x4 or x8 for 4 or 8 MHz internal clock
- Four Power Saving Modes: Halt, Active-Halt, Wait and Slow

■ Interrupt Management

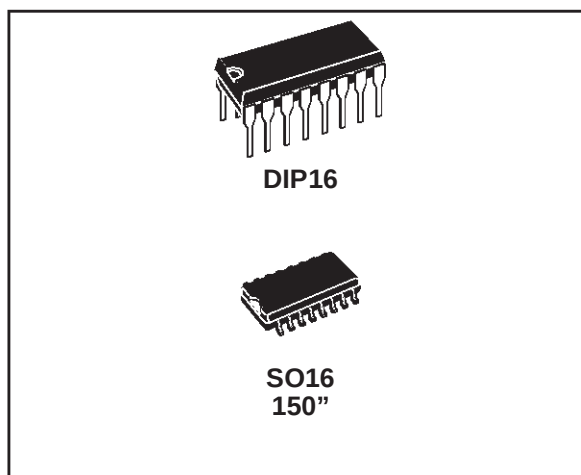
- 10 interrupt vectors plus TRAP and RESET
- 4 external interrupt lines (on 4 vectors)

■ I/O Ports

- 13 multifunctional bidirectional I/O lines
- 9 alternate function lines
- 6 high sink outputs

■ 2 Timers

- One 8-bit Lite Timer with prescaler including: watchdog, 1 realtime base and 1 input capture.
- One 12-bit Auto-reload Timer with output compare function and PWM



■ 1 Communication Interface

- SPI synchronous serial interface

■ A/D Converter

- 8-bit resolution for 0 to V_{DD}
- Fixed gain Op-amp for 11-bit resolution in 0 to 250 mV range (@ 5V V_{DD})
- 5 input channels

■ Instruction Set

- 8-bit data manipulation
- 63 basic instructions
- 17 main addressing modes
- 8 x 8 unsigned multiply instruction
- True bit manipulation

■ Development Tools

- Full hardware/software development package

Device Summary

Features	ST7FLite09	ST7FLite05
Program memory - bytes	1.5K Flash	1.5K Flash
RAM (stack) - bytes	128 (64)	128 (64)
Data EEPROM - bytes	128	-
Peripherals	Lite Timer w/ Watchdog, Autoreload Timer w/ 1 PWM, SPI, 8-bit ADC w/ Op-Amp	
Operating Supply	2.4V to 5.5V	
CPU Frequency	1MHz RC 1% + PLLx4/8MHz	
Operating Temperature	-40°C to +85°C	
Packages	SO16 150", DIP16	SO16 150", DIP16

Rev. 2.1

March 2002

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This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

1 INTRODUCTION

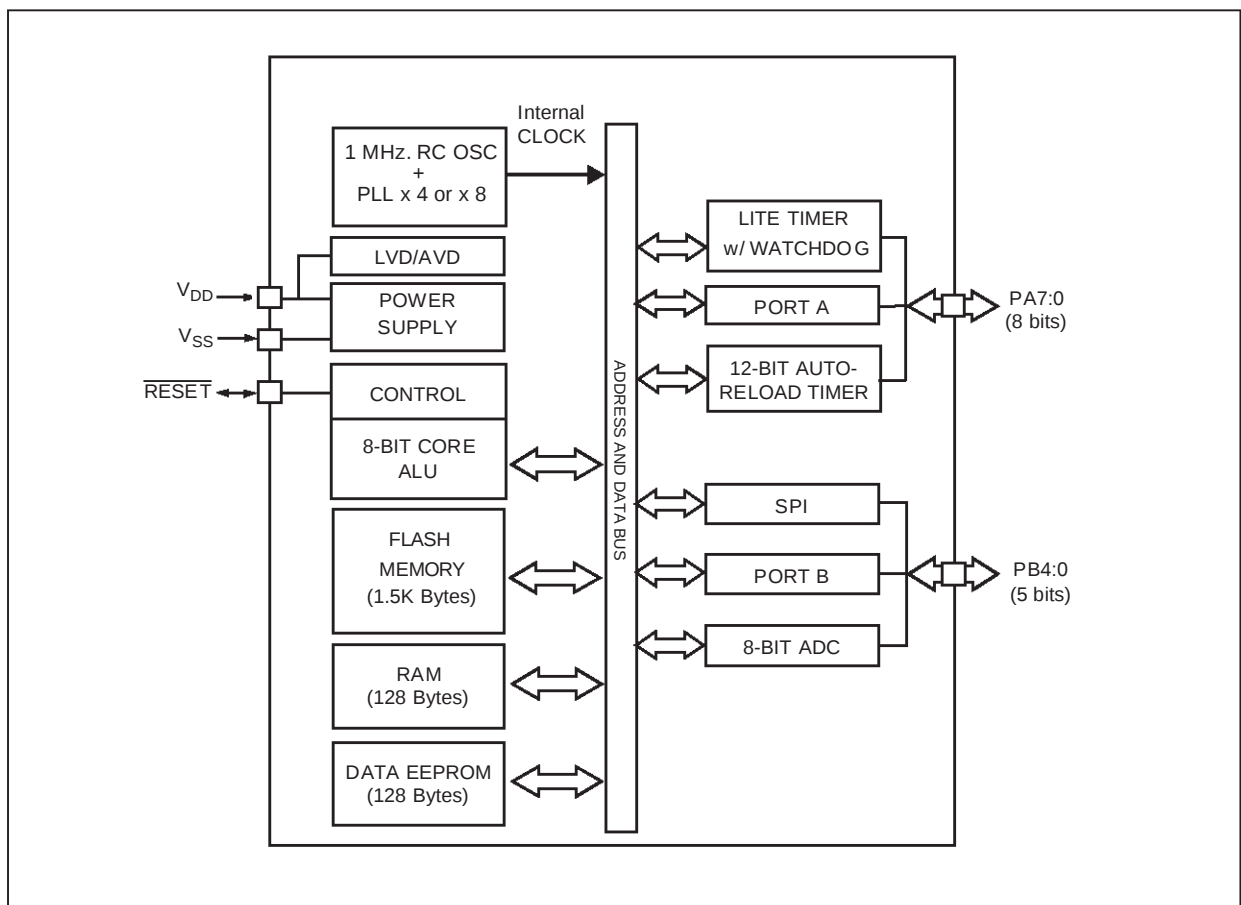
The ST7FLITE0 is a member of the ST7 microcontroller family. All ST7 devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

The ST7FLITE0 features FLASH memory with byte-by-byte In-Circuit Programming (ICP) and In-Application Programming (IAP) capability.

Under software control, the ST7FLITE0 device can be placed in WAIT, SLOW, or HALT mode, reducing power consumption when the application is in idle or standby state.

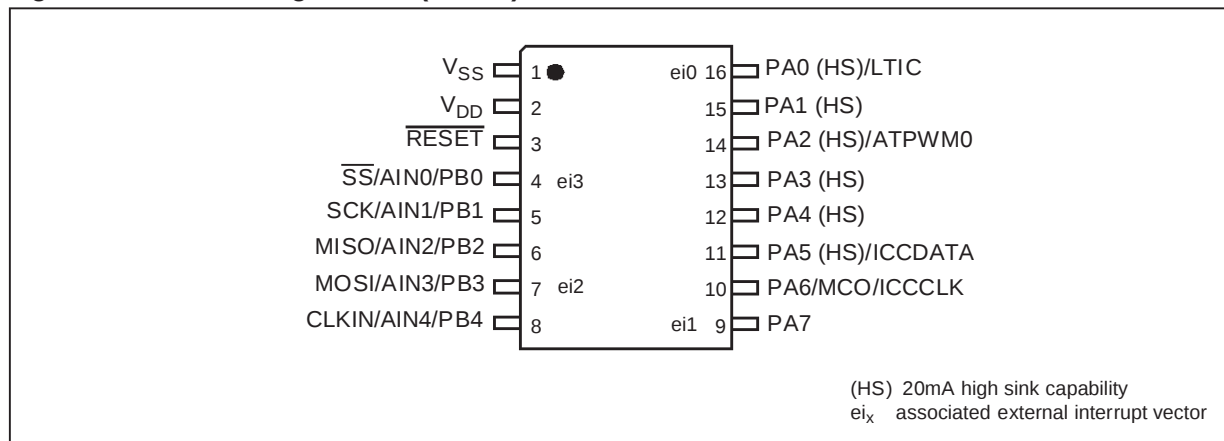
The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

Figure 1. General Block Diagram



2 PIN DESCRIPTION

Figure 2. 16-Pin Package Pinout (150mil)



PIN DESCRIPTION (Cont'd)**Legend / Abbreviations for Table 1:**

Type: I = input, O = output, S = supply

In/Output level: C= CMOS 0.15V_{DD}/0.85V_{DD} with input trigger

C_T= CMOS 0.3V_{DD}/0.7V_{DD} with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt ¹⁾, ana = analog
- Output: OD = open drain ²⁾, PP = push-pull

The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 1. Device Pin Description

Pin n°	Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function	
			Input	Output	Input				Output				
					float	wpu	int	ana	OD	PP			
1	V _{SS}	S										Ground	
2	V _{DD}	S										Main power supply	
3	RESET	I/O		C _T		X				X		Top priority non maskable interrupt (active low)	
4	PB0/AIN0/ $\overline{SS}$	I/O		C _T	X		ei3			X	X	Port B0	ADC Analog Input 0 or SPI Slave Select (active low)
5	PB1/AIN1/SCK	I/O		C _T	X	X				X	X	Port B1	ADC Analog Input 1 or SPI Serial Clock
6	PB2/AIN2/MISO	I/O		C _T	X	X				X	X	Port B2	ADC Analog Input 2 or SPI Master In/ Slave Out Data
7	PB3/AIN3/MOSI	I/O		C _T	X		ei2			X	X	Port B3	ADC Analog Input 3 or SPI Master Out / Slave In Data
8	PB4/AIN4/CLKIN	I/O		C _T	X	X				X	X	Port B4	ADC Analog Input 4 or External clock input
9	PA7	I/O		C _T	X		ei1			X	X	Port A7	
10	PA6 /MCO/ICCCLK	I/O		C _T	X	X				X	X	Port A6	Main Clock Output/In Circuit Communication Clock
11	PA5/ICCDATA	I/O	C _T	HS	X	X				X	X	Port A5	In Circuit Communication Data
12	PA4	I/O	C _T	HS	X	X				X	X	Port A4	
13	PA3	I/O	C _T	HS	X	X				X	X	Port A3	
14	PA2/ATPWM0	I/O	C _T	HS	X	X				X	X	Port A2	Auto-Reload Timer PWM0
15	PA1	I/O	C _T	HS	X	X				X	X	Port A1	
16	PA0/LTIC	I/O	C _T	HS	X		ei0			X	X	Port A0	Lite Timer Input Capture

Note:

In the interrupt input column, "ei_x" defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.

3 PACKAGE CHARACTERISTICS

3.1 PACKAGE MECHANICAL DATA

Figure 3. 16-Pin Plastic Dual In-Line Package, 300-mil Width

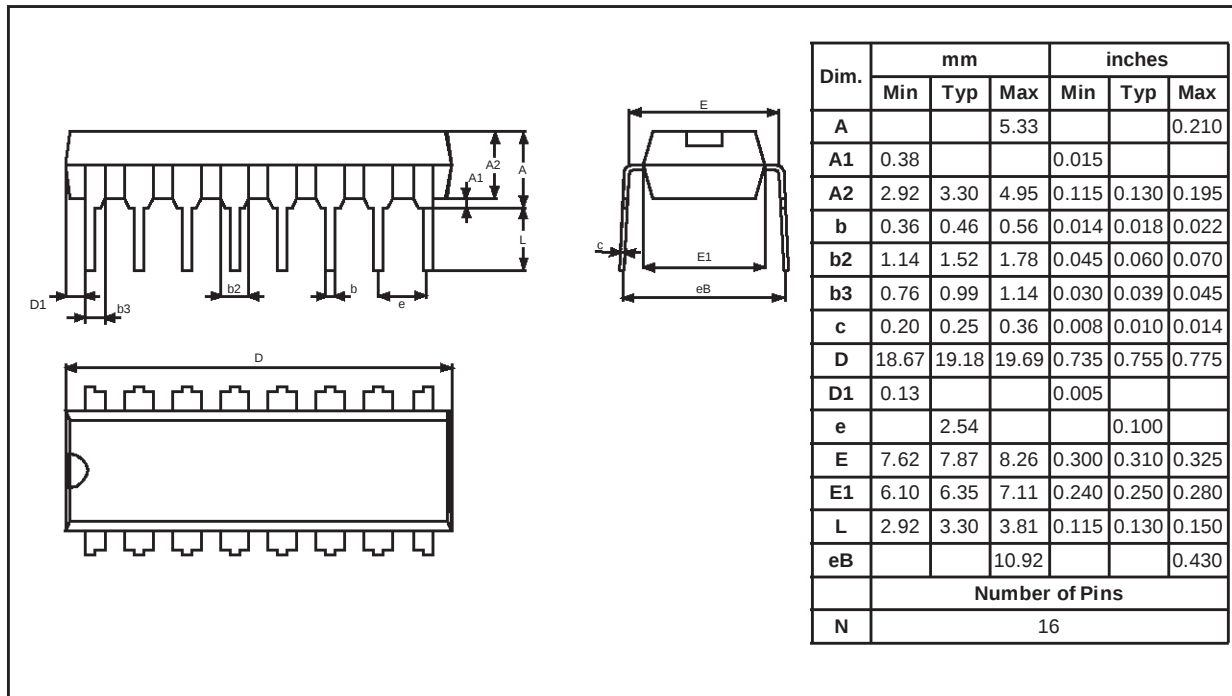
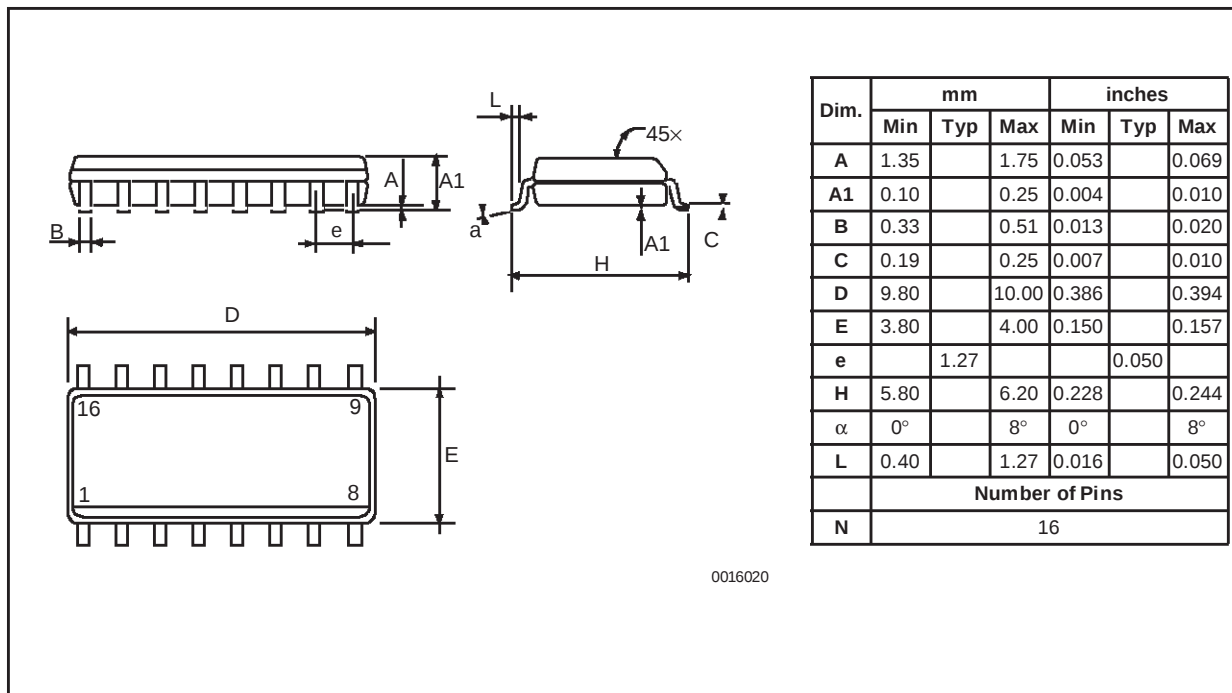


Figure 4. 16-Pin Plastic Small Outline Package, 150-mil Width



Notes:

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